What is Claimed is:

1. An output multiplexing circuit for a Double Data Rate (DDR) synchronous memory device, the output multiplexing circuit comprising:

n (where n is an integer) first latches, which simultaneously prefetch n-bit data transmitted from a memory cell array via a data path;

n first switches, which simultaneously transfer the n-bit data prefetched into the first latches to n nodes in response to a CAS latency information signal;

n second switches, which simultaneously transfer data on the nodes in response to n signals that are synchronized with a clock signal and sequentially generated at a predetermined interval;

n second latches, which store the data transferred via the second switches; and

two third switches, which sequentially transfer the data stored in the n second latches to an input terminal of an output driver of the memory device at a rising edge and a falling edge of a delay signal of the clock signal.

2. The circuit of Claim 1, wherein the predetermined interval is a half cycle of the clock signal.

3. An output multiplexing circuit for a Double Data Rate (DDR) synchronous memory device, the output multiplexing circuit comprising:

n (where n is an integer) first latches, which simultaneously prefetch n-bit data transmitted from a memory cell array via a data path;

n first switches, which simultaneously transfer the n-bit data prefetched into the first latches to n nodes in response to a CAS latency information signal;

n first logic gates, which invert the data on the nodes while an output enable signal is enabled;

n second switches, which simultaneously transfer data on the nodes in response to n signals that are synchronized with a clock signal and sequentially generated at a predetermined interval;

n second latches, which store the data transferred via the second switches;

two third switches, which sequentially transfer the data stored in the n second latches to a pull-up transistor of an output driver of the memory device at a rising edge and a falling edge of a delay signal of the clock signal;

n second logic gates, which output the data on the nodes without inverting it while the output enable signal is enabled;

n fourth switches, which sequentially transfer output signals of the second logic gates in response to the n signals;

n third latches, which store the data transferred via the fourth switches; and

two fifth switches, which sequentially transfer the data stored in the n third latches to a pull-down transistor of the output driver of the memory device at the rising edge and the falling edge of the delay signal of the clock signal.

4. The circuit of Claim 3, wherein the predetermined interval is a half cycle of the clock signal.

5. An output multiplexing method for a Double Data Rate (DDR) synchronous memory device, the output multiplexing method comprising:

simultaneously prefetching n-bit data transmitted from a memory cell array via a data path;

simultaneously transferring the prefetched n-bit data to n nodes in response to a CAS latency information signal;

transferring data on the nodes in response to n signals that are synchronized with a clock signal and sequentially generated at a predetermined interval;

storing the transferred data; and

sequentially transferring the stored data to an input terminal of an output driver of the memory device at a rising edge and a falling edge of a delay signal of the clock signal.

6. The method of Claim 5, wherein the predetermined interval is a half cycle of the clock signal.

7. An output multiplexing method for a Double Data Rate (DDR) synchronous memory device, the output multiplexing method comprising:

simultaneously prefetching n-bit data transmitted from a memory cell array via a data path;

simultaneously transferring the prefetched n-bit data in response to a CAS latency information signal;

inverting the data on the nodes while an output enable signal is enabled;

transferring the inverted data in response to n signals that are synchronized with a clock signal and sequentially generated at a predetermined interval;

storing the transferred and inverted data;

sequentially transferring the stored and inverted data to a pull-up transistor of an output driver of the memory device at a rising edge and a falling edge of a delay signal of the clock signal;

outputting the data on the nodes without inverting it while the output enable signal is enabled;

sequentially transferring the non-inverted and transferred data in response to the n signals;

storing the sequentially-transferred data; and

sequentially transferring the stored data to a pull-down transistor of the output driver of the memory device at the rising edge and the falling edge of the delay signal of the clock signal.

8. The method of Claim 7, wherein the predetermined interval is a half cycle of the clock signal.

9. An output multiplexing circuit for a memory device, the output multiplexing circuit comprising:

n (where n is an integer) first latches, which simultaneously prefetch n-bit data transmitted from a memory cell array;

n first switches, which simultaneously transfer the n-bit data that was prefetched into the n first latches to n nodes;

n second switches, which transfer data on the n nodes in response to n signals;

n second latches, which store the data transferred via the second switches; and

two third switches, which sequentially transfer the data stored in the n second latches to an output driver of the memory device at a rising edge and a falling edge of a signal.

10. An output multiplexing circuit according to Claim 9 further comprising:

n first logic gates, which invert the data on the n nodes while an output enable signal is enabled;

wherein the two third switches transfer the data stored in the n second latches to a pull-up transistor of the output driver of the memory device at a rising edge and a falling edge of the signal;

n second logic gates, which output the data on the n nodes without inverting the data, while the output enable signal is enabled;

n fourth switches, which transfer output signals of the n second logic gates in response to the n signals;

n third latches, which store the data transferred via the n fourth switches; and

two fifth switches, which sequentially transfer the data stored in the n third latches to a pull-down transistor of the output driver of the memory device at the rising edge and the falling edge of the signal.

11. An output multiplexing method for a memory device, the output multiplexing method comprising:

simultaneously prefetching n-bit data transmitted from a memory cell array;

simultaneously transferring the prefetched n-bit data to n nodes;

transferring data on the n nodes in response to n signals;

storing the data that was transferred; and

sequentially transferring the stored data to an output driver of the memory device at a rising edge and a falling edge of a signal.

12. An output multiplexing method according to Claim 11, further comprising:

inverting the data on the n nodes while an output enable signal is enabled;

wherein transferring data on the n nodes in response to n signals comprises transferring the inverted data on the n nodes in response to the n signals;

storing the transferred and inverted data;

wherein sequentially transferring the stored data to an output driver comprises sequentially transferring the stored and inverted data to a pull-up transistor of an output driver of the memory device at a rising edge and a falling edge of a signal;

outputting the data on the n nodes without inverting it while the output enable signal is enabled;

transferring the non-inverted and transferred data in response to the n signals;

storing the transferred non-inverted data; and

sequentially transferring the stored data to a pull-down transistor of the output driver of the memory device at the rising edge and the falling edge of the signal.